REMARKS

In response to a telephonic interview with the Examiner on December 17,2002, Applicants hereby submit a supplemental amendment. Applicants further submit that claims 1-11 are in condition for allowance.

The Office Action rejects originally filed claims 1-6, claims 7-11 having been filed in the previous Amendment dated June 25, 2002. Specifically, the Office Action rejects claims 1-2 and 6 as being anticipated under 35 U.S.C. § 102 by Park et al. (U.S. Patent No. 5,682,113). Claims 1, 3 and 6 stand rejected as being anticipated under 35 U.S.C. § 102 by Isobe et al. (U.S. Patent No. 4,933,579). Claims 4 and 5 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Park et al. in view of D'Souza et al. (U.S. Patent No. 5,606,270). As previously noted, the rejection of the claims over the prior art of record has been rendered moot by the amendment to independent claims 1, 6, and 11, as has the rejection of the claims depending therefrom (claims 2-5, 7-10, 12-15).

In addition to the remarks provided along with the Amendment filed, June 25, 2002, and resubmitted November 20, 2002 at the request of the Examiner, Applicants further submit that the prior art of record fails to teach or suggest, among other features of claims 1, 6 and 11, and the claims depending from those claims, including a logic circuit to which a second pulse signal output from a preceding stage inverter circuit and the inverted signal of said first pulse signal are supplied, wherein said logic circuit outputs a third pulse signal whose pulse width is changed to a second direction opposite to the first direction. The NOR gate 220 disclosed in Park et al. does not receive the second pulse signal output from a preceding stage clocked inverter circuit and the

inverted signal of said first pulse signal or output a third pulse signal whose pulse width is changed to a second direction opposite to the first direction, as claimed. Thus, at a minimum, Park et al. fails disclose each and every feature of independent claims 1, 6 and 11. Thus, claims 1-15 are in condition for allowance.

The Office Action, at page 2, asserts that Isobe et al. discloses, as illustrated in Figure 4, an apparatus comprising "a delay circuit 12 for receiving a first pulse Si, and a logic circuit (NAND gate 14) coupled to the output of the delay circuit and an inverted signal of the first pulse (via inverter 13)." The claims as amended, however, recite, in claim 6 for example, "a logic circuit to which a second pulse signal output from a preceding stage inverter circuit and the inverted signal of said first pulse signal are supplied, wherein said logic circuit outputs a third pulse signal whose pulse width is changed to a second direction opposite to the first direction." Isobe et al. does not teach or suggest the feature found in claims 1, 6 and 7. Thus, claims 1-15 are in condition for allowance.

Applicants respectfully submit that the instant application is in condition for allowance, and respectfully solicit prompt notification of the same. If any questions remain, the Examiner is invited to contact the undersigned to further prosecution.

Respectfully Submitted,

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MARKED UP VERSION OF AMENDMENT

IN THE CLAIMS

Please amend claims 1, 6 and 11 as follows.

1. (Twice Amended) A delay circuit comprising:

a clocked inverter circuit to which a first pulse signal is supplied, said clocked inverter circuit changing the pulse width of said first pulse signal in a first direction; and

a logic circuit to which a second pulse signal output from ~~said~~a preceding stage clocked inverter circuit and the inverted signal of said first pulse signal are supplied, wherein said logic circuit outputs a third pulse signal whose pulse width is changed to a second direction opposite to the first direction.

6. (Twice Amended) A delay circuit comprising:

an inverter circuit controlled by a clock signal to which a first pulse signal is supplied, said inverter circuit changing the pulse width of said first pulse signal in a first direction; and

a logic circuit to which a second pulse signal output from ~~said~~a preceding stage inverter circuit and the inverted signal of said first pulse signal are supplied, wherein said logic circuit outputs a third pulse signal whose pulse width is changed to a second direction opposite to the first direction.

11. (Amended) A delay circuit applied to a synchronizing circuit comprising:

a first delay line which includes unit delay elements and transfers a forward pulse signal;

a second delay line which includes unit delay elements and transfers a backward pulse signal; and

a state holding section which is brought into a set state or a reset state according to a transfer position of the forward pulse signal transferred along said first delay line and said

backward pulse signal transferred along said second delay line in the set state and a clock signal along said second delay line in the reset state,

wherein each of said unit delay elements constituting said first and second delay lines includes:

a clocked inverter circuit to which a first pulse signal corresponding to one of said forward and backward pulse signals output from a preceding delay unit is supplied, said clocked inverter circuit changing a pulse width of said first pulse signal in a first direction; and

a logic circuit to which a second pulse signal output from ~~said~~ a preceding stage clocked inverter circuit and an inverted signal of said first pulse signal are supplied, wherein said logic circuit outputs a third pulse signal whose pulse width is changed to a second direction opposite to the first direction.